

Searching for **hdl and address arithmetic unit and dsp**.

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[Beyond Digital Naturalism - Fontana, Wagner, Buss \(1994\)](#) (Correct) (9 citations)

The constructive aspect is essential for **addressing** both the origin problem of organizations and you-name-it. There are advocates of a single **unit** of selection, and others who claim that a www.santafe.edu/~walter/Papers/digitalnat.US.ps.gz

[Pseudec: Implementation Of The Computation-Intensive Partran.. - Finn Ller](#) (Correct)

uses redundant data representation and bitserial **arithmetic**, most significant digit first (ON-LINE than the power spectrum. Highly pipelined CORDIC-**units** optimized for the application replaces complex Equivalent To The Performance Of A Standard 10 Mips **Dsp**. The Subset Of Partran Implemented By Pseudec www.kom.auc.dk/DSP/Doc/icassp95.ps.Z

[Computer Design Strategy for MCM-D/Flip-Chip Technology - Paul Franzon](#) (Correct)

performance/cost gains are made. We also **address** the following important 'implementation '1) a 'MegaChip' CPU consisting of an Instruction Fetch **Unit** and Execution **Unit**. By building part of the www.ece.ncsu.edu/info.ece/vlsi_info/techreports/NCSU-ERL-96-03.PS.Z

[Real-Time Penalties in RISC Processing - Dropsho](#) (Correct)

the instruction buffer, instruction cache, and **address** translation hardware (TLB) Decode is self register file, data cache, TLB, and potentially **arithmetic unit** for **address** calculation. Through cache issue constraints, i.e. inter-functional **unit** dependencies. Execution must conform to data ftp.cs.umass.edu/pub/osl/papers/Penalties-TR-95-110.ps.Z

[Toward a Plan Steering Agent: Experiments with Schedule.. - Oates, Cohen \(1994\)](#) (Correct) (3 citations)

of failures while plans execute. 3) Plan steering **addresses** the problem of predicting and avoiding, in www-eksl.cs.umass.edu/papers/94-02.ps

[FREE JAZZ: A User-Level Real-Time Threads Package Designed for.. - Kramp \(1998\)](#) (Correct)

for inter-thread communication between dioeerent **address** spaces, possibly on dioeerent machines. Its This way a thread's function cushily becomes the **unit** of mutual exclusion with respect to shared data. www.uni-kl.de/AG-Nehmer/Projekte/Squirrel/postscript/tr-sfb501-9-98.ps.gz

[Code Optimization Techniques for Embedded DSP.. - Liao, Devadas.. \(1995\)](#) (Correct) (18 citations)

MA 02139 Mountain View, CA 94043 Abstract-We **address** the problem of code optimization for embedded being executed on a processor with a single **arithmetic unit** is shown. Without changing the order of (denoting the "current" AR) The **address** generation **unit** (AGU) allows the current AR to be auto-incremented ftp.inria.fr/INRIA/Projects/a3/lelait/Haiku/liao-dac95.ps.gz

[The Graham Scan Triangulates Simple Polygons - Kong, Everett, Toussaint \(1991\)](#) (Correct) (2 citations)

segments (p_i, p_{i+1}) $0 \leq i \leq n-1$, subscript **arithmetic** taken modulo n) are the edges of P . A polygon www-cgri.cs.mcgill.ca/~godfried/publications/tri.scan.ps.gz

[Optimized Software Synthesis for Digital Signal.. - Jürgen Teich.. \(1998\)](#) (Correct) (1 citation)

Summary and Conclusions 29 Abstract This paper **addresses** the problem of trading-off between the the minimal costs were computed as 15 705 memory **units**. The second graph is a randomly generated graph matter of fact, the SDF model is used in industrial **DSP** design tools, e.g. SPW by Cadence, COSSAP by ftp.tik.ee.ethz.ch/pub/people/zitzler/TZB1998a.ps.gz

[Sequential Behavior and Learning in Evolved Dynamical Neural.. - Yamauchi, Beer \(1994\)](#) (Correct) (22 citations)

reinforcement at a fixed point in time, we did not **address** the general problem of delayed reinforcement. for each neuron represented as an indivisible **unit** for the purposes of crossover. This modular vorlon.cwru.edu/~beer/Papers/seqlearn.ps.Z

[Necessary and Sufficient Conditions for Orthonormality of Scaling ... - Plonka \(1997\)](#) (Correct) (3 citations)

stability of Φ in $L^p(\mathbb{R})$ This subject is **addressed** in [3,4,12] In particular, relations between with Ω (Ω is a $r \times r$ matrix, where Ω denotes the **unit** matrix of size r). Further, the stability condition euler.math.uni-rostock.de/pub/WWW/gerlind/ortho.ps.Z

Performance Tradeoffs in Digit-Serial DSP Systems - Hiroshi Suzuki (Correct) yunchang, parhig@ece.umn.edu Abstract This paper **addresses** performance tradeoffs in digitserial **addresses** performance tradeoffs in digitserial **arithmetic** architectures for design of dedicated and block diagram of a general digit-serial **arithmetic unit** is shown in Fig. 1. Here, D represents a www.ee.umn.edu/groups/ddp/dig_ser/.../Publications/suzuki/ds_paper_asilo.ps

Development, Learning and Evolution in Animats - Kodjabachian, Meyer (1994) (Correct) (2 citations) www.biologie.ens.fr/fr/animatlab/perso/kodjaba/kjamperac.ps.gz

An Object Calculus with Algebraic Rewriting - Compagnoni, Fernández (Correct) benefit from using term rewriting to define the **arithmetic** operations instead of encoding them. 3 www.ens.fr/~maribel/papers/PLILP97.ps.gz

Statistical Learning, Localization, and Identification of... - Hornegger, Niemann (1995) (Correct) (1 citation) www5.informatik.uni-erlangen.de/TeX/Literatur/ps-dir/1995/Hornegger95:SLL.ps.gz

Fourth And Fifth Order Efficiency: Fisher Information - Kano (Correct) koko15.hus.osaka-u.ac.jp/members/kano/research/.../dvi/fisher.ps

Circulant preconditioners from B-splines - Chan, Tso, Sun (1997) (Correct) (1 citation) be the circulant matrix with diagonals that are **arithmetic** averages of the diagonals of A_n [f] extended ftp.math.cuhk.edu.hk/report/97-19.ps.Z

DSPs as flexible Multimedia Accelerators - Baumgartl, Härtig (1998) (Correct) into the instruction set and into **arithmetic** and **addressing units** resulting in an extremely powerful features into the instruction set and into **arithmetic** and **addressing units** resulting in an extremely instruction set and into **arithmetic** and **addressing units** resulting in an extremely powerful processor www.tu-chemnitz.de/~robge/ps/edrc98.ps

Scheduling Access To Temporal Data In Real-Time Databases - Xiong, Sivasankaran.. (1997) (Correct) (3 citations) The model considered is general enough to **address** one of the most important issues in real-time CPUSF t is the average time taken to get one **unit** of CPU work done. CCSF t is the slowdown factor at www-ccs.cs.umass.edu/~sim/rtdb-chapter96.ps

Frames, Objects and Relations: Three Semantic... - Norrie, Reimer.. (1994) (Correct) on large, shared knowledge bases must be **addressed**. Database systems research has focussed on www.globis.ethz.ch/publications/docs/1994d-nrlrs-krdb.ps.gz

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Searching for **hdl and address arithmetic unit and dsp**.

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No documents match Boolean query. Trying non-Boolean relevance query.

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[Approximate Kinodynamic Planning Using L 2 -norm Dynamic Bounds - Reif, Tate \(1990\)](#) (Correct) (4 citations)
 y Stephen R. Tate z Abstract In this paper we **address** the issue of kinodynamic motion planning. Given model that we use is simply a point robot with **unit** mass non-point robots can be handled easily by
www.cs.unt.edu/~srt/papers/l2motion.ps

[Mechanisms and Interfaces for Software-Extended Coherent Shared.. - Chaiken \(1994\)](#) (Correct) (3 citations)
 mechanisms including caches, location-independent **addressing**, limited directories, processor access to the (the set of processors that simultaneously access a **unit** of data) tends to be small. In fact, most blocks
ftp.cag.lcs.mit.edu/pub/papers/chaiken-dissert-1-10.ps.Z

[Analysis and Evaluation of Address Arithmetic Capabilities.. - Ashok Sudarsanam \(1997\)](#) (Correct) (13 citations)
 Analysis and Evaluation of **Address Arithmetic** Capabilities in Custom **DSP**
 Analysis and Evaluation of **Address Arithmetic** Capabilities in Custom **DSP** Architectures Ashok
 of an access graph. Offset assignment problems for **unit** increments on multiple **address** registers have been
glen.lcs.mit.edu/~devadas/pubs/cliue.ps

[Intelligent Computing About Complex Dynamical Systems - Zhao \(1994\)](#) (Correct)
 reasoning-serves as a framework for coherently **addressing** these issues and makes it possible to employ
www.cis.ohio-state.edu/insight/papers/mcs.ps

[A TMS320C40 based Speech Recognition System for Embedded.. - Obermaier, Rinner \(1998\)](#) (Correct)
 is implemented on a digital signal processor (**DSP**) of type TMS320C40 from Texas Instruments. The a prototype implementation using a TMS320C40 **DSP**. Finally, we present an experimental evaluation
 1993. 7] Texas Instruments. TMS320 Floating Point **DSP** Optimizing C Compiler. 1995. 8] Steve Young. A
www.iti.tu-graz.ac.at/en/people/rinner/.../publications/papers/obermaier98.ps.gz

[The Measurement of Textual Coherence with Latent Semantic.. - Foltz, Kintsch, Landauer \(1998\)](#) (Correct) (5 citations)
 Correspondence concerning this article should be **addressed** to Peter W. Foltz, Department of Psychology,
 LSA provides a fully automatic method for comparing **units** of textual information to each other in order to
lsa.colorado.edu/papers/dp2.foltz.ps

[Further Illustration Of The Use Of The.. - De Mirleau](#) (Correct)
 A x) r /B y) 0 3 3 We will not **address** the question whether this condition can be
 2.1. Let A be a symmetric associative algebra with **unit** and typical elements f g, let L :Der(A) with
preprints.cern.ch/archive/electronic/hep-th/9703/9703061.ps.gz

[The Formalisation of a Hardware Description Language in a Proof.. - Goossens \(1993\)](#) (Correct)
 Abstract Hardware description languages (**hdl**s) are a notation to describe behavioural and
 an aspect of a circuit description which is not **addressed** in the semantics (e.g. layout area) the two
 a trademark of the Secretary of State for Defence, **United Kingdom**. 3 Lambda is a product of Abstract
ftp.dcs.ed.ac.uk/pub/kgg/lfcsreport269.ps.Z

[Learning Planning Operators by Observation and Practice - Wang \(1994\)](#) (Correct) (12 citations)
 Abstract The work described in this paper **addresses** learning planning operators by observing
 expressed or implied, of Wright Laboratory or the **United States Government**. The learning system is given
www.rpal.rockwell.com/~mei/aips94.ps

[Formalising Abilities and Opportunities of Agents - van Linder, van der Hoek, Meyer \(1998\)](#) (Correct) (2 citations)
 and workshops were initiated that specifically **address** agents, their theories, languages, architectures
ftp.cs.uu.nl/pub/RUU/CS/techreps/CS-1998/1998-08.ps.gz

[Models for Asynchronous Message Handling - Langendoen, Bhoedjang, Bal \(1997\)](#) (Correct) (4 citations)
 from user space to avoid or eliminate expensive **address**-space crossings. Using such architectures,

ftp.cs.vu.nl/pub/amoeba/orca_papers/ieee-concurrency97.ps.gz

The System Of Two Spinning Disks In The Torus. - Wojtkowski (1993) (Correct)
only if (7) 1 2 2 With these formulas we can **address** the question of linear stability in the system
periodic orbits with all Floquet exponents on the **unit** circle. We would like to thank Eugene Gutkin and
mpej.unige.ch/mp_arc/c/94/94-88.ps.gz

Using PVM 3.0 to Run Grand Challenge Applications on.. - Dongarra, Geist.. (1992) (Correct)
computational Grand Challenge problems are being **addressed** at Oak Ridge National Laboratory. Two examples
<ftp.netlib.org/ncwn/siam93-pvmgc.ps>

Low Latency Word Serial CORDIC - Villalba, Lang (1997) (Correct)
In [6] the double rotation method for redundant **arithmetic** and rotation mode is proposed, where two
this estimate we have used the following delays in **units** of the delay of a full adder (Tfa) shifter: 2.5
<ftp.ac.uma.es/pub/reports/1997/UMA-DAC-97-05.ps.gz>

Topic Detection and Tracking Pilot Study - Allan, Carbonell, Doddington.. (1998) (Correct)
the approaches used by the study members to **address** the problem of text segmentation and discusses
Second, the word seems like a more suitable **unit** of measurement, because of the relatively high
www.cs.cmu.edu/~yiming/papers.yy/tdt1-final-report.ps

Working Memory and Dyslexia - Fawcett, Baddeley (1992) (Correct)
underlie both sets of symptoms. This issue was **addressed** via a series of experiments designed to
*Department of Psychology MRC Applied Psychology **Unit** University of Sheffield Cambridge Abstract Recent
<ftp.shef.ac.uk/pub/uni/projects/scp/lrgdocs/lrg913.ps>

Segregatory Coordination and Ellipsis in Text Generation - Shaw (1998) (Correct) (6 citations)
and Sag, 1994 Carpenter, 1998) We will not **address** common problems associated with parsing, such as
coordination, the coordination of smaller **units** is logically equivalent to coordination of
www.cs.columbia.edu/~shaw/papers/colingac198.ps.gz

Exploiting SIMD Parallelism in DSP and Multimedia Algorithms.. - Nguyen, John (1999) (Correct) (5 citations)
while expanding the processor's capabilities to **address** high-bandwidth data processing and intensive
inverse discrete cosine transforms, and vector **arithmetic**. Each algorithm has one non-AltiVec version,
by providing a 128-bit vector execution **unit**, which operates concurrently with the existing
www.ece.utexas.edu/projects/ece/lca/ps/ics.ps

Decision-Making On Fuzzy Pieces Of Evidence - Schuster, Adamson, Bell (Correct)
is too high then further measurements of LDL and HDL cholesterol are required [Slyper, 1994] The two
www.ifs.tuwien.ac.at/~silvia/idamap99/idamap99-13.pdf

Foreign Event Handlers to Maintain Information Consistency and.. - Queloz (1999) (Correct)
University of Geneva, Switzerland, E-mail **address**: PierreAntoine.Queloz@cui.unige.ch Broadly
cuiwww.unige.ch/~queloz/papers/mac3.1999.ps.gz

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Searching for **address arithmetic unit and dsp and auto update**.

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[Analysis and Evaluation of Address Arithmetic Capabilities..](#) - Ashok Sudarsanam (1997) (Correct) (13 citations)

Analysis and Evaluation of **Address Arithmetic** Capabilities in Custom **DSP**

Analysis and Evaluation of **Address Arithmetic** Capabilities in Custom **DSP** Architectures Ashok

of an access graph. Offset assignment problems for **unit** increments on multiple **address** registers have been
glen.lcs.mit.edu/~devadas/pubs/cliue.ps

[Evaluating the Effect of Auto-update on the Kendall Square KSR1](#) - Karim Harzallah (Correct)

includes four architectural features that **address** the memory latency problem: i) **automatic** average access time of the second phase is the **arithmetic** mean of all access times during this phase. cell consists of an integer and floating point **unit**, 0.25 MB instruction and data subcache, 32 MB
ftp.cs.toronto.edu/pub/reports/csrg/291/291.ps.Z

[Exploiting SIMD Parallelism in DSP and Multimedia Algorithms..](#) - Nguyen, John (1999) (Correct) (5 citations)

while expanding the processor's capabilities to **address** high-bandwidth data processing and intensive inverse discrete cosine transforms, and vector **arithmetic**. Each algorithm has one non-AltiVec version, by providing a 128-bit vector execution **unit**, which operates concurrently with the existing
www.ece.utexas.edu/projects/ece/lca/ps/ics.ps

[Storage Assignment to Decrease Code Size](#) - Liao (1995) (Correct) (36 citations)

DSP architectures typically provide indirect **addressing** modes with **auto**-increment and decrement. In to use **address** registers and perform **address arithmetic** to access **automatic** variables. Subsuming the problem. Given an undirected graph H , we assign a **unit** weight to each edge. Now a Hamiltonian path exists
glen.lcs.mit.edu/~devadas/pubs/toplas.ps

[A Uniform Optimization Technique for Offset Assignment Problems](#) - Leupers, David (1998) (Correct) (2 citations)

layout of local variables in memory, such that the **addresses** of variables can be computed efficiently in such AGUs permit to execute two types of **address arithmetic** operations in parallel to other instructions:

DSPs are equipped with **address** generation **units** (AGUs) capable of performing indirect **address**

ls12-www.cs.uni-dortmund.de/publications/papers/1998-iss_b.ps.gz

[Scheduling Access To Temporal Data In Real-Time Databases](#) - Xiong, Sivasankaran.. (1997) (Correct) (3 citations)

The model considered is general enough to **address** one of the most important issues in real-time CPUSF t is the average time taken to get one **unit** of CPU work done. CCSF t is the slowdown factor at of time. Examples of such applications include **autopilot** systems, robot navigation, and program stock
www-ccs.cs.umass.edu/~sim/rtdb-chapter96.ps

[Storage Assignment using Expression Tree Transformations to..](#) - Rao, Pande (Correct)

architectures typically provide dedicated memory **address** generation **units** and indirect **addressing** modes and decrement that subsume **address arithmetic**. The heavy use of **auto**-increment and provide dedicated memory **address** generation **units** and indirect **addressing** modes with **auto**-increment
www.eecs.uc.edu/~arao/public_papers/interact3.ps

[Storage Assignment Optimizations to Generate Compact and..](#) - Rao, Pande (1999) (Correct) (3 citations)

architectures typically provide dedicated memory **address** generation **units** and indirect **addressing** modes and **auto**-decrement that subsume **address arithmetic** calculation. The heavy use of **auto**-increment provide dedicated memory **address** generation **units** and indirect **addressing** modes with **auto**-increment
www.eecs.uc.edu/~santosh/pldi99.ps

[An Object Calculus with Algebraic Rewriting](#) - Compagnoni, Fernández (Correct)

benefit from using term rewriting to define the **arithmetic** operations instead of encoding them. 3 -calculus. The untyped λ calculus supports method **update**. The first-order (typed) version of the calculus, for objects whose methods return self or an **updated** version of self. With these extensions, the
www.ens.fr/~maribel/papers/PLILP97.ps.gz

Approximate Kinodynamic Planning Using L2-norm Dynamic Bounds - Reif, Tate (1990) (Correct) (4 citations)
y Stephen R. Tate z Abstract In this paper we **address** the issue of kinodynamic motion planning. Given model that we use is simply a point robot with **unit** mass non-point robots can be handled easily by Planning, IEEE Int. Conf. on Robotics and Automation, 1989, pp. 958-963. 5] B. Donald and P. www.cs.unt.edu/~srt/papers/l2motion.ps

Frames, Objects and Relations: Three Semantic.. - Norrie, Reimer.. (1994) (Correct)
on large, shared knowledge bases must be **addressed**. Database systems research has focussed on that they support efficient retrieval and **update** operations on large, shared knowledge bases. is used as a simple storage system with query and **update** strategies controlled primarily at the object www.globis.ethz.ch/publications/docs/1994d-nrlrs-krdb.ps.gz

System Support for Software Fault Tolerance in Highly Available.. - Sullivan (1992) (Correct) (3 citations)
It observes a higher availability impact from **addressing** errors, such as uninitialized pointers, than wuarchive.wustl.edu/packages/postgres/papers/ERL-M93-05.ps.Z

DSPs as flexible Multimedia Accelerators - Baumgartl, Härtig (1998) (Correct)
into the instruction set and into **arithmetic** and **addressing units** resulting in an extremely powerful features into the instruction set and into **arithmetic** and **addressing units** resulting in an extremely instruction set and into **arithmetic** and **addressing units** resulting in an extremely powerful processor www.tu-chemnitz.de/~robge/ps/edrc98.ps

Novel Code Optimization Techniques for DSPs - Leupers (1998) (Correct) (1 citation)
techniques: maximum utilization of parallel **address** generation **units**, exploitation of is any "regular" machine instruction, e.g. an **arithmetic** operation, a register move, or a jump. The maximum utilization of parallel **address** generation **units**, exploitation of instruction-level parallelism ls12-www.cs.uni-dortmund.de/publications/papers/1998-dsper.ps.gz

Code Optimization Techniques for Embedded DSP.. - Liao, Devadas.. (1995) (Correct) (18 citations)
MA 02139 Mountain View, CA 94043 Abstract-We **address** the problem of code optimization for embedded being executed on a processor with a single **arithmetic unit** is shown. Without changing the order of (denoting the "current" AR)The **address** generation **unit** (AGU) allows the current AR to be **auto**-incremented ftp.inria.fr/INRIA/Projects/a3/lclait/Haiku/liao-dac95.ps.gz

Pseudec: Implementation Of The Computation-Intensive Partran.. - Finn Ller (Correct)
uses redundant data representation and bitserial **arithmetic**, most significant digit first (ON-LINE than the power spectrum. Highly pipelined CORDIC-**units** optimized for the application replaces complex Equivalent To The Performance Of A Standard 10 Mips Dsp. The Subset Of Partran Implemented By Pseudec www.kom.auc.dk/DSP/Doc/icassp95.ps.Z

Algorithms for Address Assignment in DSP Code Generation - Leupers, Marwedel (1996) (Correct) (15 citations)
DESIGN (ICCAD)1996, c fIEEE 1 Algorithms for **Address** Assignment in **DSP** Code Generation Rainer We define a generic model of **DSP address** generation **units**. Based on this model, we present efficient c fIEEE 1 Algorithms for **Address** Assignment in **DSP** Code Generation Rainer Leupers, Peter Marwedel ls12-www.cs.uni-dortmund.de/publications/papers/1996-iccad.ps.gz

A Structural Approach For Designing Performance Enhanced .. - Weiss, Walther, Fettweis (Correct)
Load/store Instruction Words .Load/store (2 X)**Address** Generation (2 X)2 2 Total Number Of Isa Fus e.g. by allowing concurrent memory accesses and **arithmetic** calculations. However, to efficiently support Thus, a common strategy is to replicate **arithmetic units** or implement tailored datapaths. Both methods www.ifn.et.tu-dresden.de/~weissm/paper/icassp97_paper.ps.gz

Mechanisms and Interfaces for Software-Extended Coherent Shared.. - Chaiken (1994) (Correct) (3 citations)
mechanisms including caches, location-independent **addressing**, limited directories, processor access to the (the set of processors that simultaneously access a **unit** of data) tends to be small. In fact, most blocks with and without help from programmers. An **automatic** optimization technique transmits information ftp.cag.lcs.mit.edu/pub/papers/chaiken-dissert-1-10.ps.Z

Foreign Event Handlers to Maintain Information Consistency and.. - Queloz (1999) (Correct)
University of Geneva, Switzerland, E-mail **address**: PierreAntoine.Queloz@cui.unige.ch Broadly in the Context of Competition and Cooperation -**Autonomous Agents Conference** -1999 y Centre allow external software entities to retrieve and **update** information or to watch events occuring in the cuiwww.unige.ch/~queloz/papers/mac3.1999.ps.gz

Searching for **user defined addressing mode and hdl**.

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[An evaluation of the effectiveness of the C compiler for the.. - Joseph Buck \(Correct\)](#)

The Amount Of Time The Sparc Cpu Spent Executing **User** Code The Time For System Code Was Excluded. for high-level languages other than C)There are **definite** advantages to choosing C as the language to Most **modern** DSPs include a circular buffer **addressing mode** to accomplish (in a virtual sense) the ptolemy.eecs.berkeley.edu/~parks/papers/cs252-s90.ps.gz

[Modeling and Simulation of Electromechanical.. - Romanowicz.. \(1997\) \(Correct\)](#)

in bond-graph theory. The flow variable is **defined** as the time derivative of the state or

Modeling and Simulation of Electromechanical

method. All **models** of transducers are written in **HDL-A TM** a proprietary analogue hardware

galahad.informatik.tu-chemnitz.de/proceedings/edtc/papers/1997/edt97/htmlfiles/sun_sgi/.../pdffiles/02d_3.pdf

[Generalizations of the Sethi-Ullman algorithm for register.. - Appel, Supowit \(1987\) \(Correct\) \(6 citations\)](#)

for generalized Sethi-Ullman numbers We thus **define** a generalized computation tree as one in which example of a multiregister value comes from the **addressing modes** of the VAX. The operands of an add Certain computations can be appropriately **modelled** as computation trees. A computation tree has www.cs.princeton.edu/~appel/papers/sun.ps

[Low Latency Word Serial CORDIC - Villalba, Lang \(1997\) \(Correct\)](#)

on the merged equations (3) shown in section 2, we **define** a new system of equations making the change of working both in rotation and vectoring operation **modes**, presenting a low latency in comparison with the ftp.ac.uma.es/pub/reports/1997/UMA-DAC-97-05.ps.gz

[Pragmatic Issues in Handling Miscommunication: Observations of .. - Ronnie Smith \(1996\) \(Correct\) \(2 citations\)](#)

caused by misstatements by the human **user**. After overviewing the operational environment of with this system indicate that in a well-**defined** problem domain (1) many miscommunications can they occur. Our domain **model** is fairly complex, **addressing** twelve different features of the LED under www.cs.ecu.edu/faculty/smith/www/papers/aaai96wrk.ps

[Online Aggregation - Hellerstein, Haas, Wang \(1997\) \(Correct\) \(73 citations\)](#)

returned. This archaic approach is frustrating to **users** and has been abandoned in most other areas of in a system called approximate [VL93]This system **defines** an approximate relational algebra which it uses discuss a number of system issues that need to be **addressed** in order to best support this sort of control db.cs.berkeley.edu/papers/sigmod97-online.ps.Z

[Failure Mode Assumptions and Assumption Coverage - David Powell \(1992\) \(Correct\) \(29 citations\)](#)

by a system (or a component 1 to a single **user**. This **model** specifies the service as the sequence on the validity of such assumptions. Formal **definitions** are given for the types of errors that can 1 Failure **Mode** Assumptions and Assumption Coverage David ftp.laas.fr/pub/Publications/1991/91462.ps

[Large Object Support in POSTGRES - Stonebraker, Olson \(1993\) \(Correct\) \(4 citations\)](#)

the POSTGRES abstract data type paradigm, support **userdefined** operators and functions, and allow objects in the database. The support for **user-defined** storage managers available in POSTGRES is also systems [BATO86, HAAS90, STON90]Proposals have **addressed** the inclusion of new types, new access methods, s2k-ftp.cs.berkeley.edu:8000/sequoia/tech-reports/s2k-93-30/s2k-93-30.ps.Z

[Performance Comparison Of Video Transport Over ATM.. - Hossain, Kang, Horst \(Correct\)](#)

each of these two interconnects. The appropriate **user-level** packet sizes for the served video are also are created)Each descriptor contains the **address** of these 4KByte data which need to be digital video over ATM (Asynchronous Transfer **Mode**) and ServerNet (from Tandem Computers Inc.We berserk.vlsi.uiuc.edu/people/ashfaq/ieee.mm97.ps

- user defined addressing mode and hdl ResearchIndex document query
- Intelligent Computing About Complex Dynamical Systems - Zhao (1994) (Correct)
- finding for performing the simulation task human **users** need to prepare the simulation and to interpret describes a control design task in terms of well-defined geometric, combinatorial operations on the flow reasoning-serves as a framework for coherently **addressing** these issues and makes it possible to employ www.cis.ohio-state.edu/insight/papers/mcs.ps

Code Optimization Techniques for Embedded DSP.. - Liao, Devadas.. (1995) (Correct) (18 citations)
 schedule P_i such that $jP_i \leq jL$, where L is a **user**-specified parameter in the range $2 \leq L \leq jV_j$. The
 of these schedules is called a reduced schedule. **Definition 1:** Let S_p and S_q be valid reduced schedules
 MA 02139 Mountain View, CA 94043 Abstract-We **address** the problem of code optimization for embedded
ftp.inria.fr/INRIA/Projects/a3/lelait/Haiku/liao-dac95.ps.gz

Using Kernel Extensions to Decrease the Latency of User-Level.. - Riesen (1996) (Correct)
 Using Kernel Extensions to Decrease the Latency of **User**-Level Communication Primitives University of New
ftp.cs.unm.edu/pub/cs_tech_reports/1996/prop.ps.gz

FREE JAZZ: A User-Level Real-Time Threads Package Designed for.. - Kramp (1998) (Correct)
 Free Jazz: An **User**-Level Real-Time Threads Package Designed for
 for inter-thread communication between different **address** spaces, possibly on different machines. Its
 thread lists and scheduling, context switching **modes**, stack management, as well as timing and
www.uni-kl.de/AG-Nehmer/Projekte/Squirrel/postscript/tr-sfb501-9-98.ps.gz

Retargetable Generation of Code Selectors from HDL Processor.. - Leupers, Marwedel (1997) (Correct) (9 citations)
 styles. The processor **model** visible to the **user** is an **HDL model**. This **model** optionally
 code for different target processors (within a **defined** processor class) in such a way that the largest
 load-store & memory-register post-modify **addressing modes** register structure heterogeneous &
ls12-www.cs.uni-dortmund.de/publications/papers/1997-edtc.ps.gz

System-Level Specification of Instruction Sets - Todd Cook (1993) (Correct) (2 citations)
 endtask endmodule ftp.cs.chalmers.se/pub/users/harcourt/iccd93.ps.gz
 an implementation detail since it is not **defined** by the ISA. Instruction Formats. LISAS provides
 costs and design time is also at this stage [4]**Addressing** these issues requires accurate, concise
ftp.cs.chalmers.se/pub/users/harcourt/iccd93.ps.gz

Sub-element Indexing and Probabilistic Retrieval in the POSTGRES .. - Fontaine (1995) (Correct) (1 citation)
 that a particular document is relevant to the **user's** information need as expressed in a natural
 on components extracted from both builtin and **user-defined** abstract data types. In conventional indexes the
 as probabilistic retrieval, are being explored to **address** some of these problems. Probabilistic retrieval
wuarchive.wustl.edu/packages/postgres/papers/CSD-95-876.ps.Z

TrIAs - An Architecture for Trainable Information Assistants - Bauer, Dengler (1998) (Correct) (3 citations)
 to perform certain tasks on behalf of their **users**. In many cases, however, the agent's competence
 of documents, full specification and use of **user-defined** abstractions (macros) full homogeneous language
 applying recognizers, and **defining** macros are **addressed**. The Interaction Style The basic goal is to
www.dfki.de/~bauer/aaai-ws-10.ps

Disk System Design for Guaranteeing Quality of Service in.. - Chih-Yuan Cheng (1998) (Correct) (1 citation)
 validity of the queueing **model**. This paper also **addresses** the related implementation issues. Keywords:
 support a stream switching from the normal playback **mode** to a fast search **mode** while providing VCR-like
moon.csie.ntu.edu.tw/pub/publications/1997/spie98-1.ps.gz

North American ISDN Users' Forum Application Software Interface .. - Part Ms-Dos (Correct)
 North American ISDN **Users'** Forum Application Software Interface (ASI) Part
 5.0. Callback Function **Definitions**
 3.0. **Address** Resolution Device
isdn.ncsl.nist.gov/niuf/404-92-2.ps

Recovering Active Databases - Zukunft (1995) (Correct) (1 citation)
 that they only change their state or respond to **users** if they receive an external stimulus. An active
 database operations, time signalisations and **user-defined** events. The condition usually consists of a
 These techniques result in a modified and coupling **mode** specific algorithm for the detection of complex
ftp.informatik.uni-oldenburg.de/pub/tech-reports/TR-IS-AIS-03-95.ps.gz

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